

Amendments to the claims:

Claims 1-8 (canceled)

Claim 9 (currently amended): ~~The method of claim 8 wherein:~~

A method for making a semiconductor device comprising:

forming a dielectric layer on a substrate;

forming a metal layer on the dielectric layer;

forming on the metal layer a masking layer that has first and second sides;

lining the first and second sides of the masking layer with a sacrificial layer;

~~the metal layer is etched by~~ applying a plasma dry etch process to etch a first part of the metal layer, and applying a wet etch process to etch a second part of the metal layer;

applying a wet etch process ~~is applied~~ to etch the dielectric layer; and

applying a wet etch process ~~is applied~~ to remove the sacrificial layer.

Claims 10-16 (canceled)

Claim 17 (currently amended): ~~The method of claim 16 wherein:~~

A method for making a semiconductor device comprising:

forming a dielectric layer on a substrate;

forming a first metal layer on a first part of the dielectric layer, leaving a second part of the dielectric layer exposed;

forming a second metal layer on the first metal layer and on the second part of the dielectric layer;

forming on the second metal layer a masking layer that has first and second sides;

lining the first and second sides of the masking layer with a sacrificial layer;

~~the second metal layer and the first metal layer are etched by~~ applying a plasma dry etch process to etch a first part of the second metal layer and a first part of the first metal layer, and applying a wet etch process to etch a second part of the second metal layer and a second part of the first metal layer;

~~applying~~ a wet etch process is applied to etch the dielectric layer; and

~~applying~~ a wet etch process is applied to remove the sacrificial layer.

Claim 18 (canceled)

Claim 19 (currently amended): ~~The method of claim 18 wherein:~~

A method for making a semiconductor device comprising:

forming a high-k gate dielectric layer on a substrate;

forming a first metal layer on the high-k gate dielectric layer;

removing part of the first metal layer;

forming a second metal layer on the first metal layer and on the high-k gate dielectric layer, a first part of the second metal layer covering the remaining part of the first metal layer and a second part of the second metal layer covering the high-k gate dielectric layer;

forming a polysilicon layer on the second metal layer;

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removing part of the polysilicon layer to generate a patterned polysilicon layer that has first and second sides, and to expose a third part of the second



~~polysilicon layer to generate a patterned polysilicon layer that has first and second sides, and to expose a third part of the second~~

removing part of the polysilicon layer to generate a patterned polysilicon layer that has first and second sides, and to expose a third part of the second metal layer;

depositing a the sacrificial layer that comprises a material that is selected from the group consisting of silicon nitride, a carbon doped silicon nitride, and silicon dioxide;~~the first and second sides of the patterned polysilicon layer are lined with the sacrificial layer by depositing the sacrificial layer onto the second metal layer, and onto the first and second sides of the patterned polysilicon layer, then applying an anisotropic plasma dry etch process to remove the sacrificial layer from the second metal layer; and further comprising:~~

~~removing the exposed third part of the second metal layer and the underlying part of the first metal layer after lining the first and second sides of the patterned polysilicon layer with the sacrificial layer; and~~

~~removing the sacrificial layer after the exposed third part of the second metal layer and the underlying part of the first metal layer are removed.~~